

REMARKS

Claim 8 was objected to because of an informality. Claim 8 has been rewritten to overcome the rejection.

Claims 1, 2, 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Murouchi, U.S. Patent No. 6,067,144, in view of Mathew et al., U.S. Patent No. 6,122,033. Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over Murouchi in view of Ishikawa et al., U.S. Patent No. 6,414,733. Claims 7-9 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Murouchi and Ishikawa et al., and further in view of Ogura et al., U.S. Patent No. 5,739,888. Claims 3-5, 12, 14, and 15-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Murouchi and Mathew et al., and further in view of Mashiko et al., U.S. Patent No. 6,288,766.

Applicant respectfully disagrees with the contention of the Examiner that Mathew et al. discloses the ratio of the contact area between the column spacers and the other of the substrate structures to the total area occupied by the plural pixels being within the range from 0.030 percent to 0.120 percent.

Although, it is true that the diameter of the spacers in Mathew et al., is between 2-4 micrometers, and the length/width of the pixels are approximately 100 micrometers, as stated in column 1, lines 32-35 of Mathew et al., it does not follow that the contact area between the spacers and the substrate structure is 3-12 square micrometers as indicated by the Examiner, (Office Action, page 3, lines 5-8). It is to be noted that the spacers 8 disclosed in Mathew et al. are stated to be typically spherical in shape. Thus, the contact area between such spacers and glass plates 2 and 4, (see Fig. 1b), ranges between a point contact to some undetermined amount of area less than the full cross-sectional area of the spacers 8, based upon the pressure exerted on

the spacers 8 by the glass plates 2 and 4. There is thus no basis for the assumption of the Examiner that the contact area is between 3-12 square micrometers which seems to be approximately a cross-sectional area of each of the spacers.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

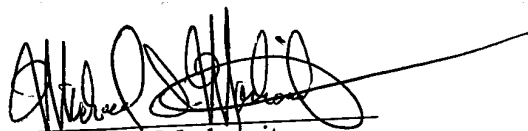
CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on
Deposit Account 50-1290.

Respectfully submitted,


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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph covering the entirety of page 17 has been rewritten as follows:

The diameter D1 of the spherical spacers 22 is theoretically given as

$$D1=(A+B+2C+D+E+F+G) [. H. B. E. F.G] \underline{-H-B-E-F-G}$$

$$=A+D+2C [. H] \underline{-H} \text{ (micron)} \quad (1)$$

where A is the thickness of the color filter 16 in micron, B is the thickness of the overcoat layer 11 in micron, C is the thickness of the orientation layer 9 in micron, D is the height of the column spacer 41 in micron, E is the thickness of the passivation layer 8 in micron, F is the thickness of the gate insulating layer 7 in micron, G is the thickness of the gate electrode 1 in micron and H is the thickness of the black matrix 17 in micron. The height D is measured from the boundary between the color filter 16 and the overcoat layer 11 to the boundary between the orientation layers 9. In actual products of the IPS liquid crystal display panel, the spherical spacers 22 are partially embedded in the overcoat layer 11 under the black matrix 17, and the spherical spacers 22 are designed in such a manner as to have the diameter D1' equal to or less than (D1 + 2) microns. Equation (1) is given on the assumption that there is a conductive layer patterned concurrently to the scanning lines 1 under the spherical spacers 22. If the gate insulating layer 7 is directly held in contact with the inner surface of the transparent insulating substrate 6a under the spherical spacers 22, the diameter [D1] D2 is given as

$$D2=(A+B+2C+D+E+F+G) [. H. B. E.F] \underline{-H-B-E-F}$$

$$= A+D+2C+G [. H] \underline{-H} \text{ (micron)} \quad (2)$$

Even so, the spherical spacers 22 are designed in such a manner as to have the diameter D1' equal to or less than (D1 + 2) microns.

The paragraph on page 18, lines 1-8, has been rewritten as follows:

The polarizing plates 19 have the transmitting directions of polarized light shown in figure 3. In this instance, the angle $\theta 1$ is 75 degrees, and the angle $\theta 2$ is - 15 degrees. Thus, the relative relation between the polarizing plates 19 is similar to that of the prior art IPS [liqu9id] liquid crystal display panel. The orientation layers 9 were rubbed, and the direction of rubbing on the active matrix substrate structure 46 is substantially in parallel to the direction of rubbing on the counter substrate structure 43, and the direction of rubbing crosses the direction $\theta 3$ of electric field at 75 degrees, i.e., $\theta 1$.

IN THE CLAIMS

Claims 1, 8, and 15 have been rewritten as follows:

1. (Once Amended) A liquid crystal display panel comprising
a pair of substrate structures having plural pixels where an image is produced,
liquid crystal filling a gap between the substrate structures of said pair and selectively
making said pixels dark and bright for producing said image, and
column spacers formed on one of said substrate structures of said pair and held in contact
with the other of said substrate structures, the ratio of the total contact area between said column
spacers and said other of said substrate structures to the total area occupied by said plural pixels
being [fallen] within the range from 0.050 percent to 0.150 percent.
8. (Once Amended) The liquid crystal display panel as set forth in claim 7, in which said
spacers are spherical and have a diameter expressed as

$$DM = (A + B + 2C + D + E + F + G) - H - B - E$$

$$[- G] - \underline{F} - \underline{G} = A + D + 2C - H$$

where DM is the diameter of said spacers in micron, A is a thickness of color filters formed on said one of said substrate structures in micron, B is a thickness of an overcoat layer covering said color filters in micron, C is a thickness of orientation layers respectively covering said overcoat layer and a passivation layer over said switching transistors and said pixel electrodes in micron, D is a height of said column spacers in micron, E is a thickness of said passivation layer in micron, F is a thickness of a gate insulating layer forming parts of said switching transistors in micron, G is a thickness of gate electrodes forming other parts of said switching transistors in micron and H is a thickness of a black matrix covered with said color filters in micron.

15. (Once Amended) A process for fabricating a liquid crystal display panel, comprising the steps of:

- a) preparing a pair of substrate structures having column spacers;
- b) assembling the substrate structures of said pair in alignment with one another for creating a gap therebetween;
- c) injecting liquid crystal into said gap;
- d) evacuating part of said liquid crystal from said gap so [a] as to make a pressure exerted on the inner surfaces of said substrate structures lower than the atmospheric pressure; and
- f) confining the remaining part of said liquid crystal in said [gap.] gap.

in which said column spacers formed in one of said substrate structures are held in contact with the other of said substrate structures for creating said gap, and the ratio of total contact area between said column spacers and said other of said substrate structures to the area occupied by pixels is within the range between 0.050% to 0.150%.